

APPROVED BY
DRAFTSMAN
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PATENT & TRADEMARK OFFICE
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BLAKELY, SOKOL OF TAYLOR & ZAFMAN LLP (303) 740-1980
Title: Executing Parallel Width Packed Data Instructions
Inventors: Mohammed Abdallah, et al.
Filing Date: May 8, 2001
Application No.: 09/852,217
Sheet: 1 of 13 Attorney Docket No: 42390P5193C

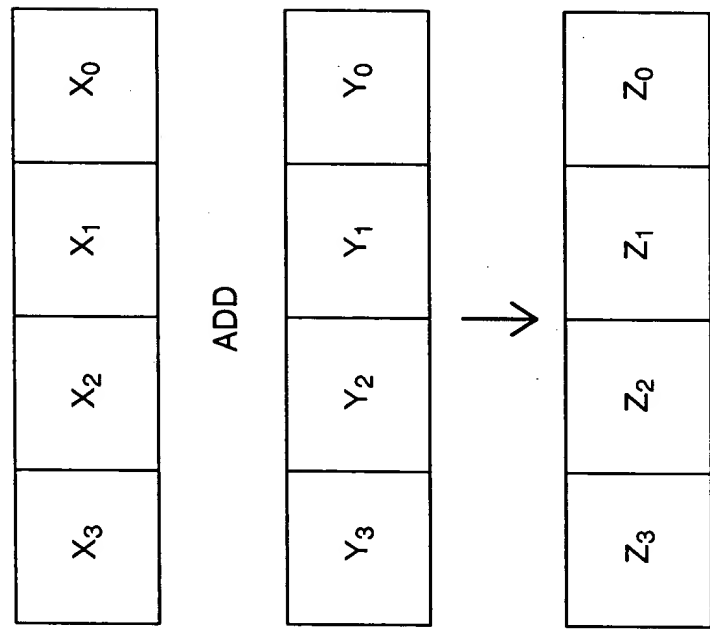


FIG. 1
PRIOR ART

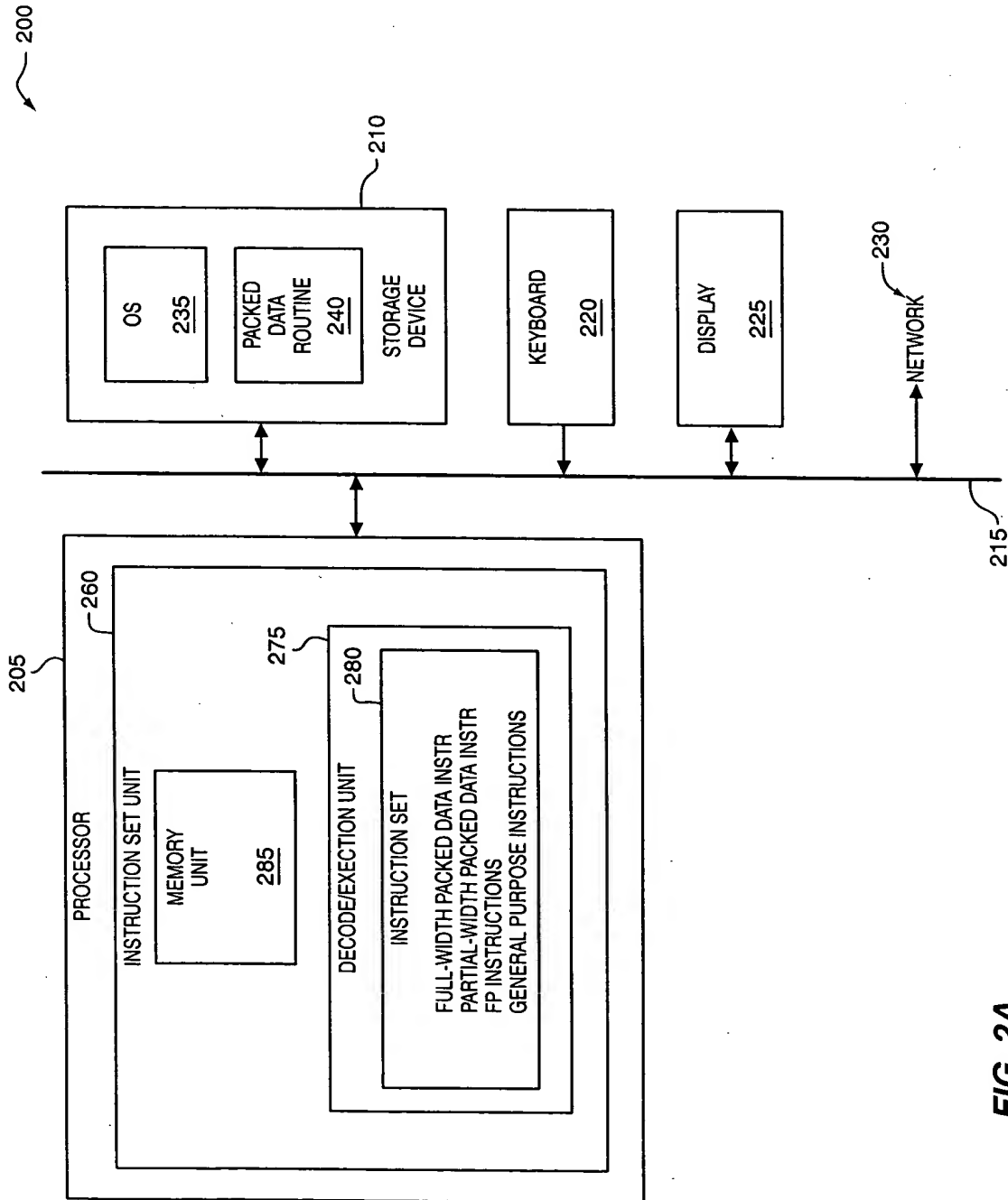
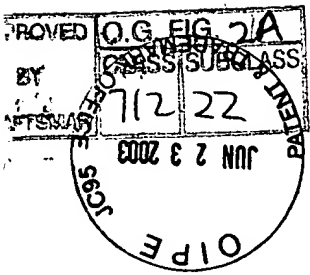


FIG. 2A

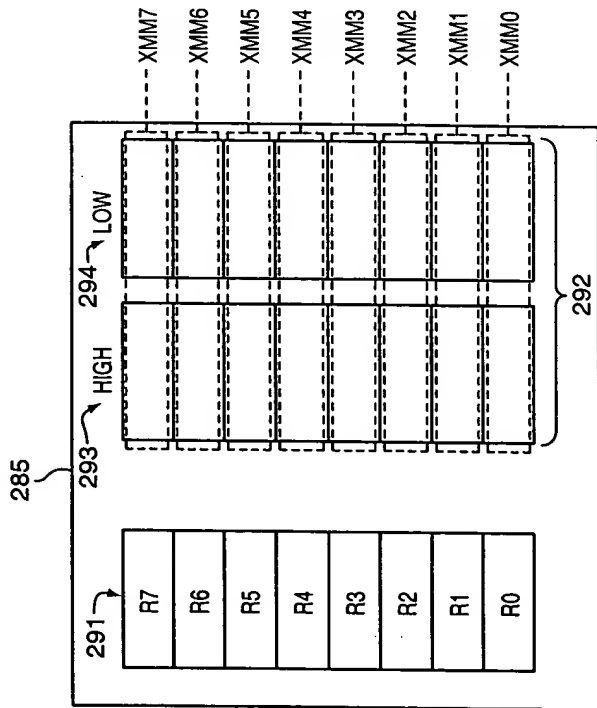
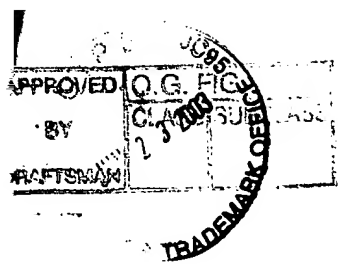


FIG. 2C

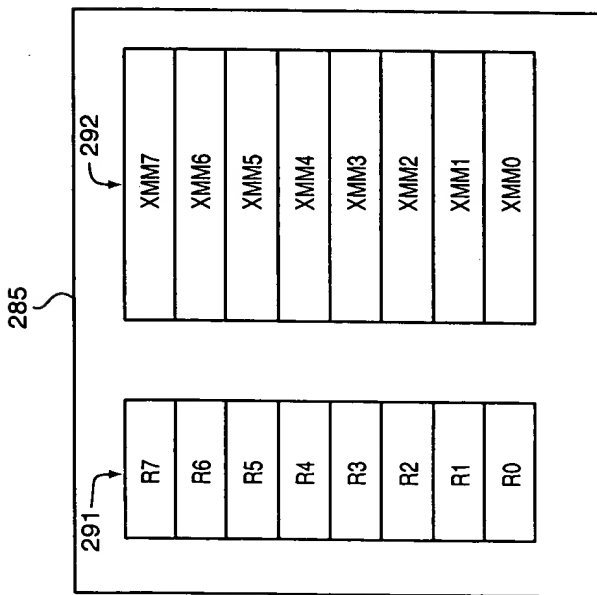


FIG. 2B

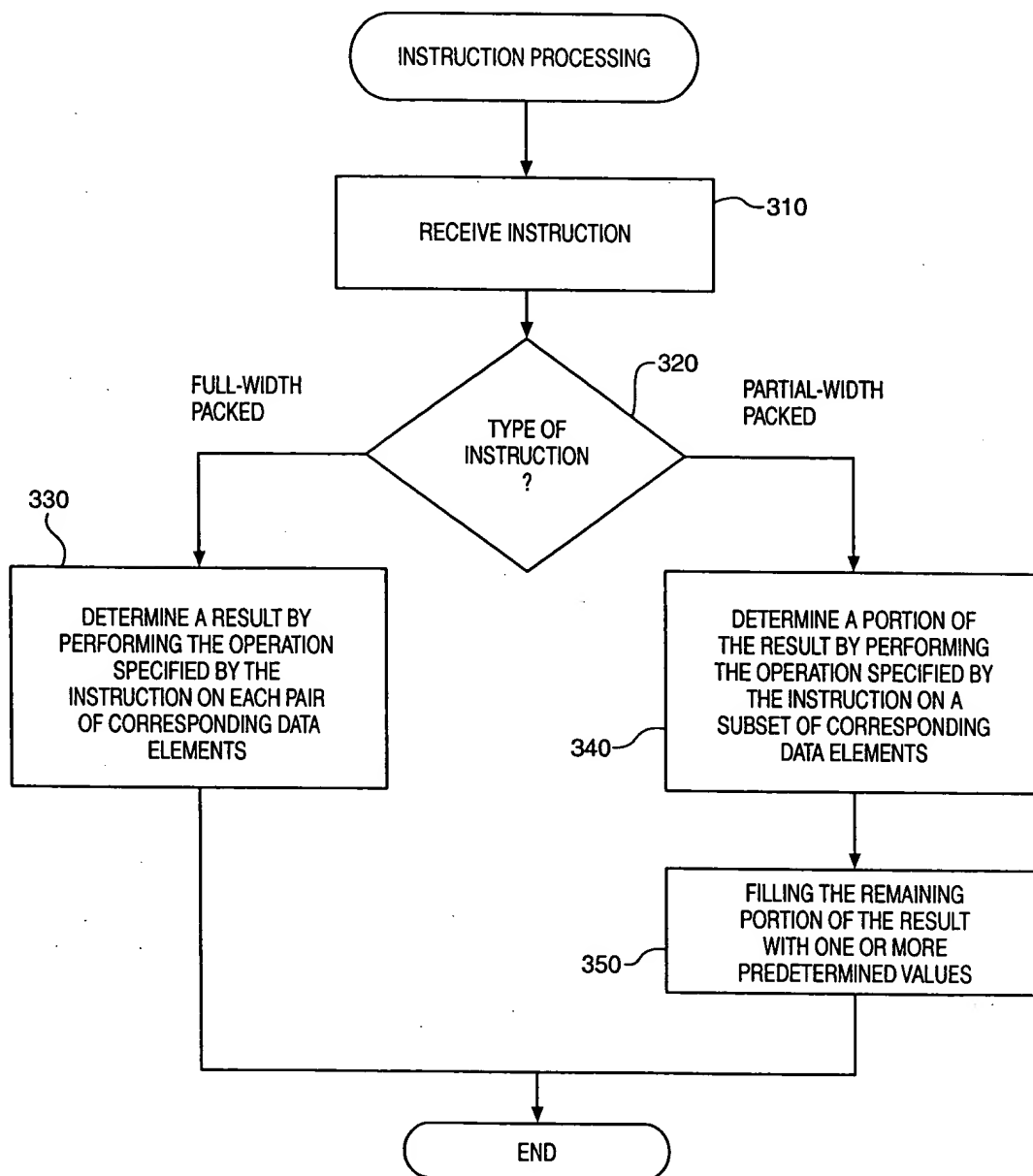
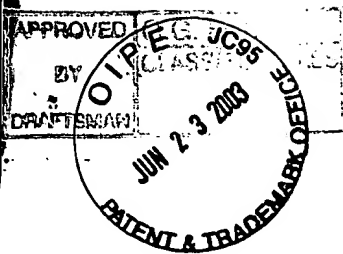


FIG. 3

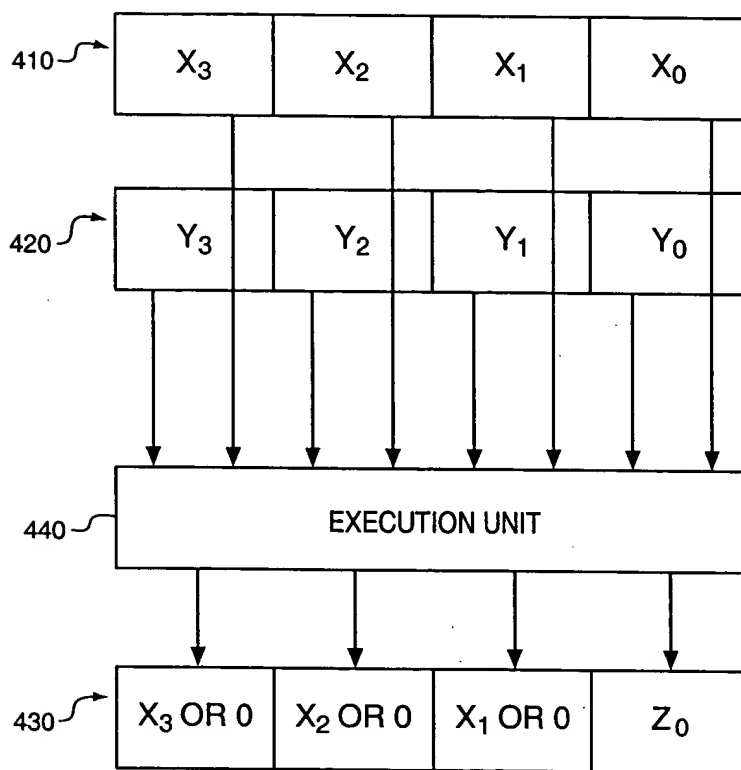


FIG. 4

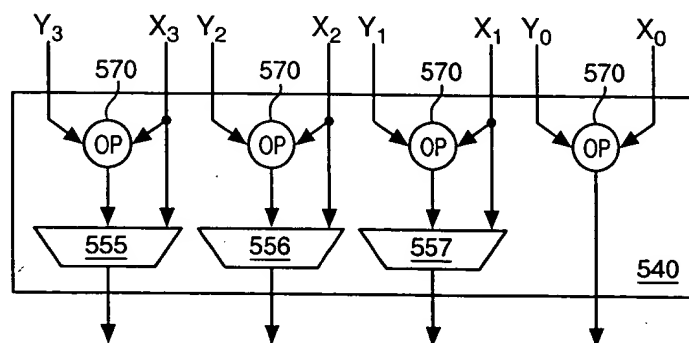
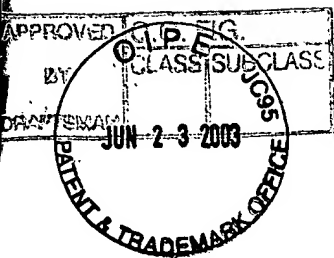


FIG. 5A

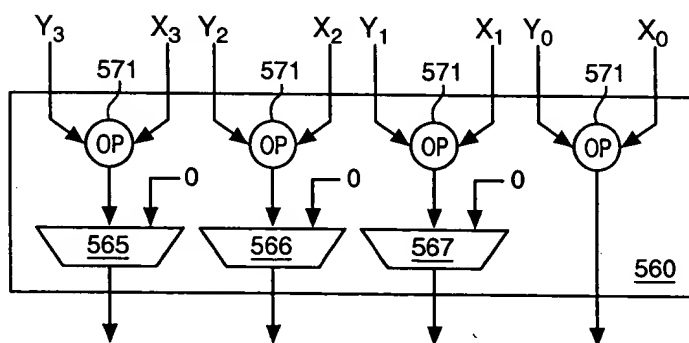


FIG. 5B

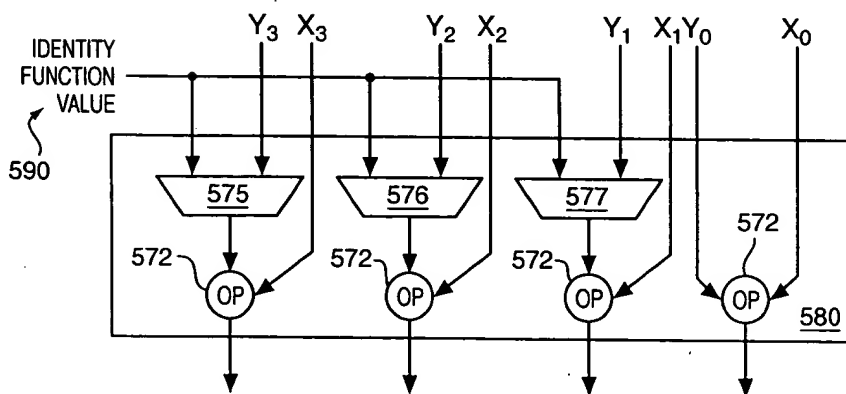
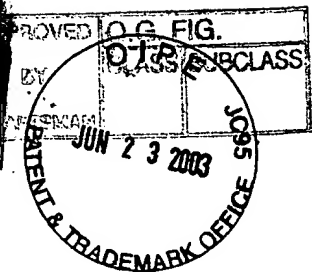


FIG. 5C



BLAKELY, SOKOLOFF, TORRES & ZAFMAN LLP (303) 740-1980
Title: Executing Partially Packed Data Instructions
Inventors: Mohammed Abdallah, et al.
Filing Date: May 8, 2001
Application No.: 09/852,217
Sheet: 7 of 13 Attorney Docket No: 42390P5193C

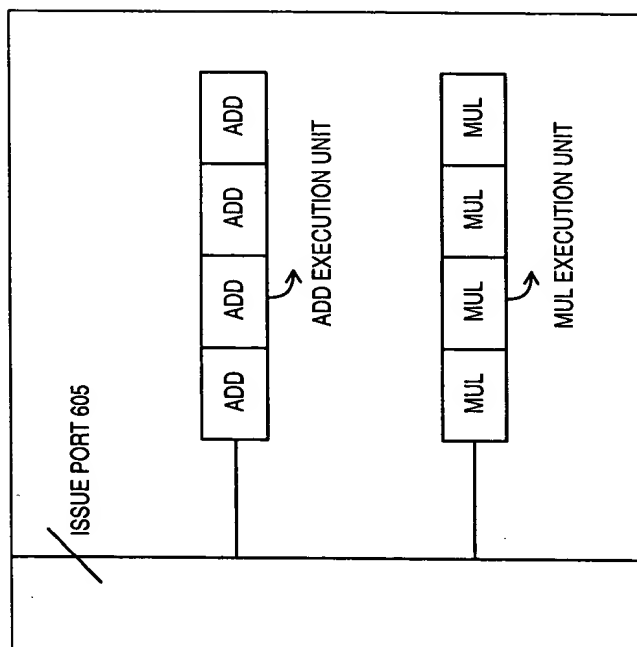
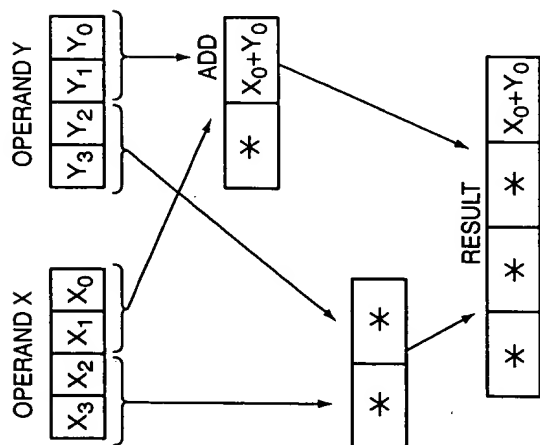
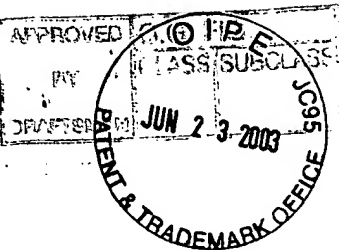


FIG. 6



* = CORRESPONDING DATA ELEMENT
 IN X OR Y, NaN, 0, OR OTHER
 PREDETERMINED VALUE

FIG. 7B

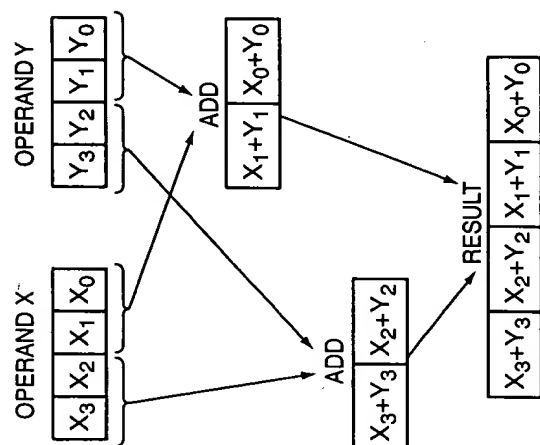


FIG. 7A

TIME

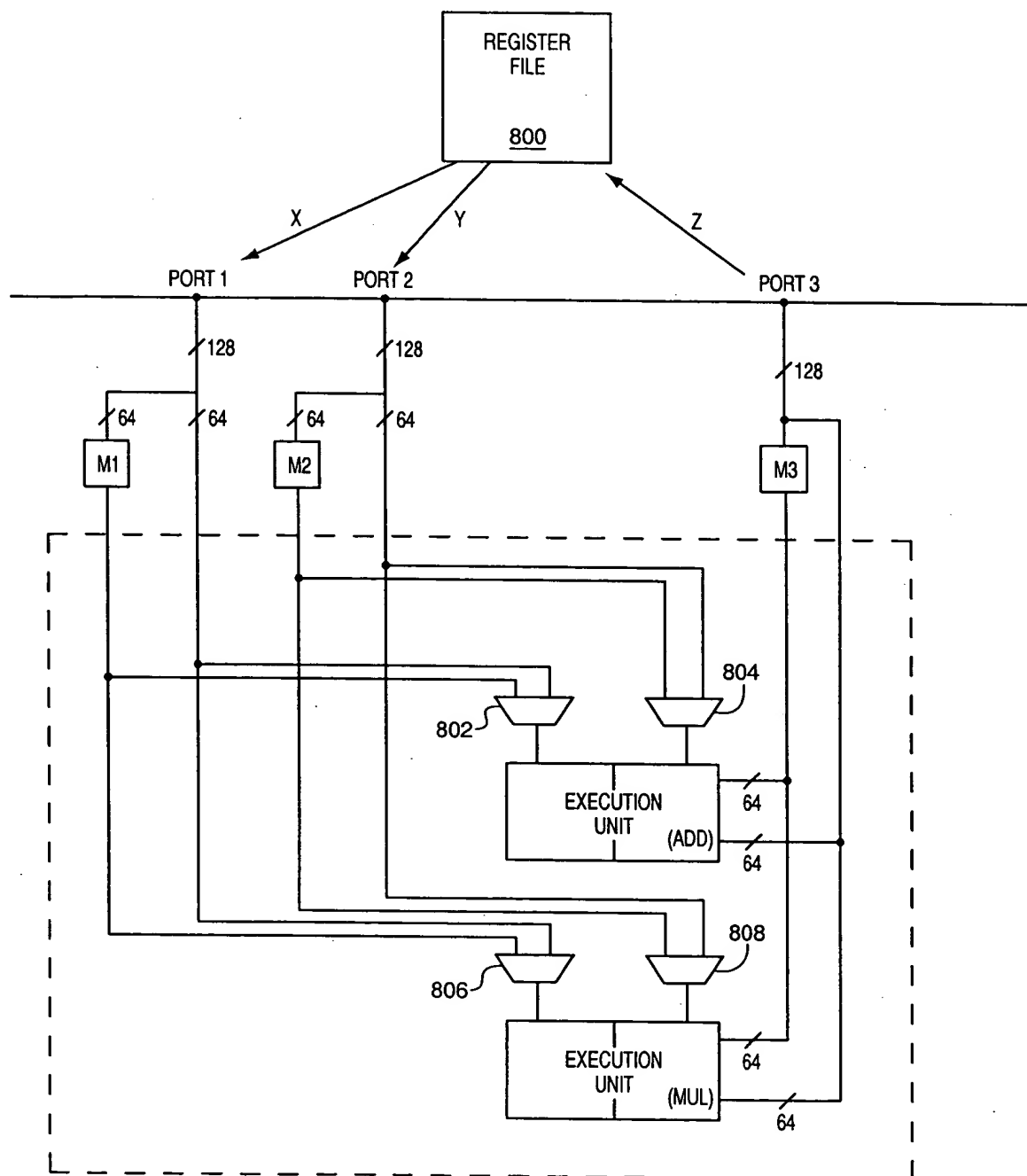
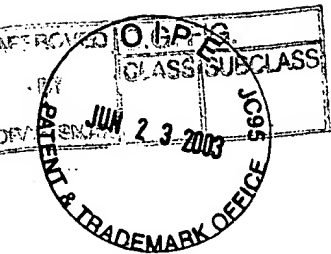
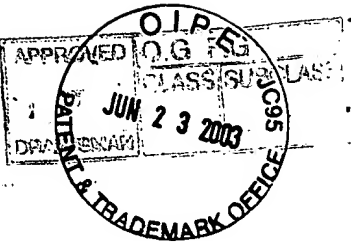


FIG. 8A



TIME	128-BIT INSTRUCTION	PERFORMED ON 64-BIT DATA
T	ADD X, Y	ADD X ₀ Y ₀ ADD X ₁ Y ₁
T+1		ADD X ₂ Y ₂ ADD X ₃ Y ₃
T+1	MUL X, Y	MUL X ₀ Y ₀ MUL X ₁ Y ₁
T+2		MUL X ₂ Y ₂ MUL X ₃ Y ₃

FIG. 8B

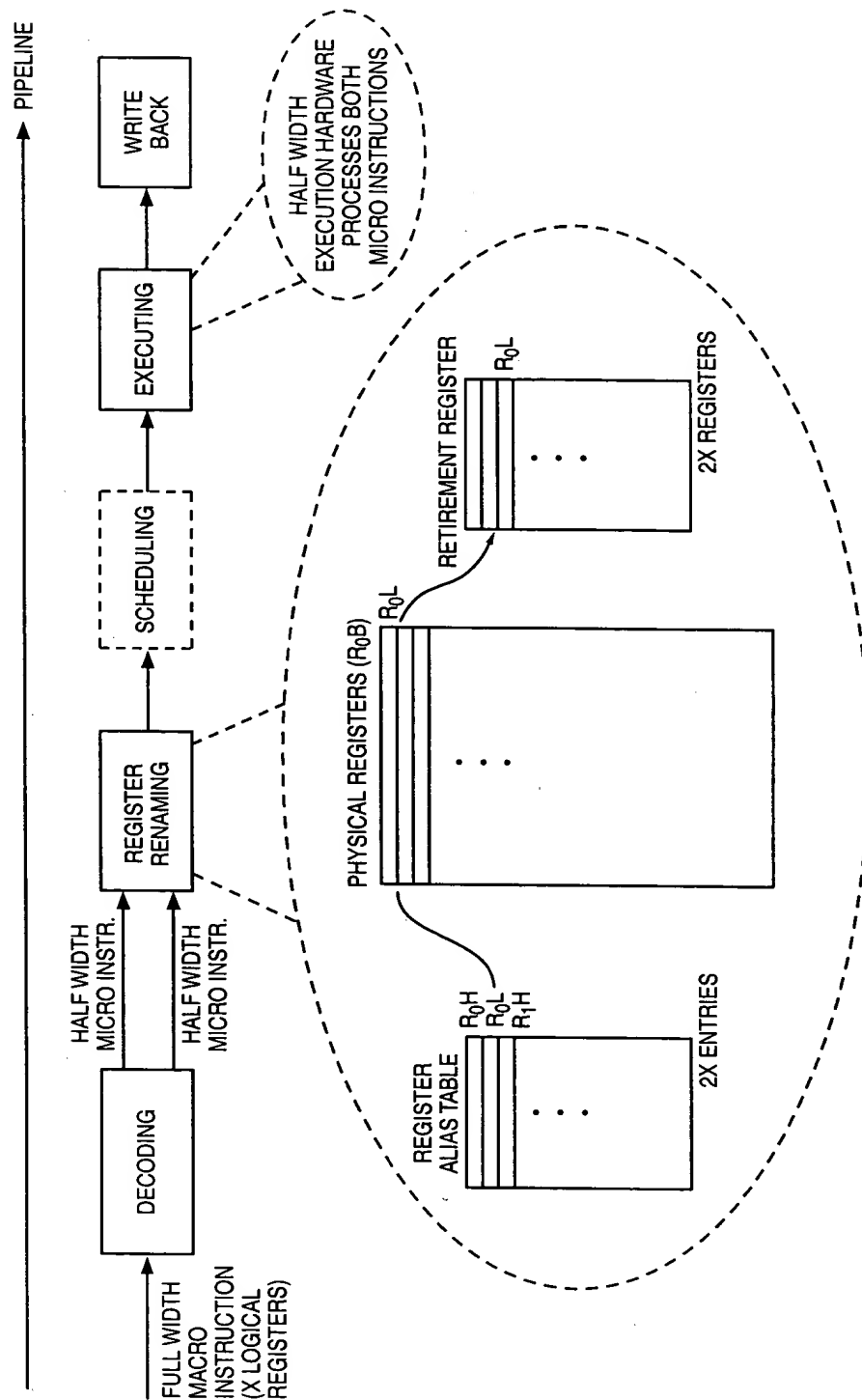
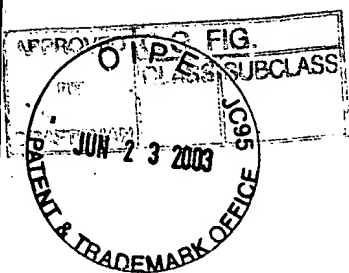
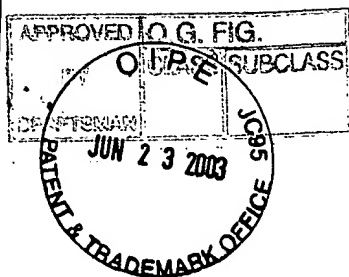


FIG. 9



BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP (303) 740-1980
Title: Executing Partial-Width Packed Data Instructions
Inventors: Mohammed Abdallah, et al.
Filing Date: May 8, 2001
Application No.: 09/852,217
Sheet: 12 of 13 Attorney Docket No: 42390P5193C

TIME	128-BIT INSTRUCTION	64-BIT INSTRUCTION
T	ADD X, Y	ADD X_L, Y_L
T + N		ADD X_H, Y_H

FIG. 10

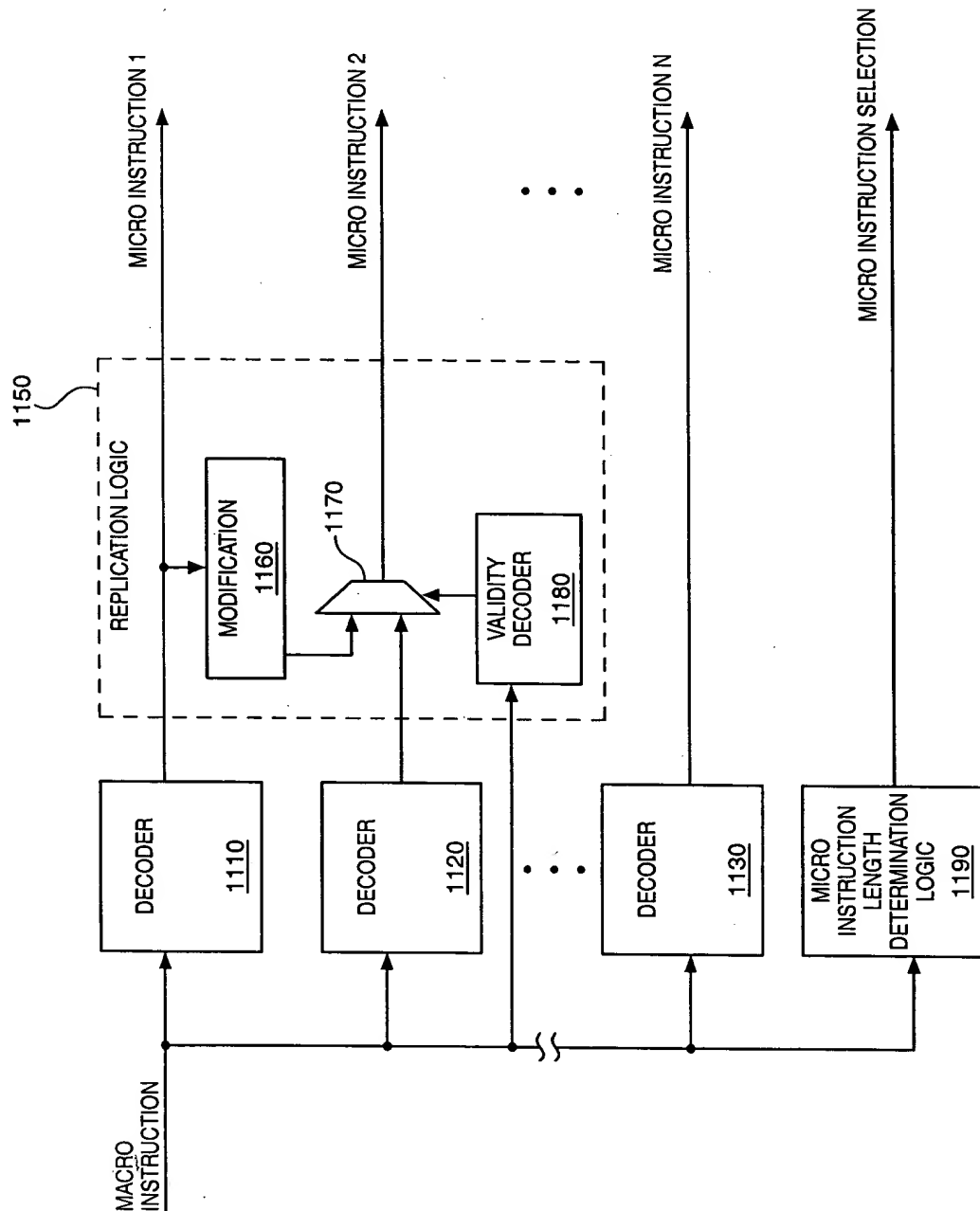
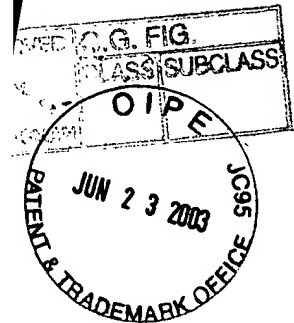


FIG. 11